We claim:

1. A method of reducing power consumption in a data receiver, the receiver being configured to process a received signal using repeated implementations of substantially the same first data processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element, the method comprising:

determining a number of repetitions of said repeated implementations of said first data processing element;

processing said receiving signal according to said determined number of repetitions;

adjusting said number of repetitions in response to a power saving control signal; and

jointly reducing said clock frequency and a power supply voltage to said first data processing element in response to said control signal to reduce said receiver power consumption.

2. A method as claimed in claim 1 wherein the receiver is configured to process said signal in substantially real time, and wherein said receiver power consumption is reduced whilst maintaining said substantially real time processing capability.

3. A method as claimed in claim 1 wherein said receiver has a subsequent data processing element configured to input data from said repeated implementations of said first data processing element, and wherein the method further comprises writing data from said repeated implementations of said first data processing element into a store and asynchronously reading said data from said repeated implementations of said first data processing element from said store prior to providing said data to said subsequent data processing element.

4. A method as claimed in claim 1 wherein said control signal is responsive to one or more of a desired or determined received signal quality, a noise and/or interference level, and a desired power consumption parameter.

5. A method as claimed in claim 1 wherein said joint reducing of said clock frequency and power supply voltage comprises selecting a clock frequency and power supply voltage combination from a set of clock frequency-supply voltage combinations stored in the receiver.

6. A method as claimed claim 1 further comprising:

increasing said number of repetitions in response to a second control signal; and

jointly increasing said clock frequency and said power supply voltage in response to said second control signal.

7. A method as claimed in claim 1 wherein said receiver is a rake receiver and said first data processing element comprises at least a time multiplexed correlator for said rake receiver.

8. A method as claimed in claim 1 wherein said first data processing element comprises a time multiplexed rake finger for said rake receiver.

9. A method as claimed in claim 1 wherein said first data processing element comprises at least a portion of a turbo equaliser or turbo-decoder.

10. A method as claimed in claim 1 wherein said data processing element comprises an interference canceller for said receiver.

11. A method as claimed in claim 1 wherein said data processing element comprises a finite impulse response filter or equaliser for said receiver.

12. A method as claimed in claim 1 wherein said data processing element comprises a maximum likelihood sequence estimator channel equaliser for said receiver.

13. Processor control code to, when running, implement a method of reducing power consumption in a data receiver, the receiver being configured to process a received signal using repeated implementations of substantially the same first data

processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element, the method comprising:

determining a number of repetitions of said repeated implementations of said first data processing element;

processing said receiving signal according to said determined number of repetitions;

adjusting said number of repetitions in response to a power saving control signal; and

jointly reducing said clock frequency and a power supply voltage to said first data processing element in response to said control signal to reduce said receiver power consumption.

14. A data carrier carrying the processor control code of claim 13.

15. A power controller for a data receiver, the receiver being configured to process a received signal using repeated implementations of substantially the same first data processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element, the power controller comprising:

means for determining a number of repetitions of said repeated implementations of said first data processing element;

means for adjusting said number of repetitions in response to a power saving control signal; and

means for jointly reducing said clock frequency and a power supply voltage to said first data processing element in response to said control signal to reduce said receiver power consumption.

16. A power controller as claimed in claim 15 wherein said receiver has a subsequent data processing element configured to input data from said repeated implementations of said first data processing element, and wherein the controller further comprises a buffer configured for storing said data from said repeated implementations of said first data processing element and configured to permit reading of said data from said repeated implementations of said first data processing element asynchronously with said storing, for provision to said subsequent data processing element.

17. A power controller as claimed in claim 15 wherein said receiver is a rake receiver and said first data processing element comprises at least a time multiplexed correlator for said rake receiver, preferably a time multiplexed rake finger for said rake receiver.

18. A receiver including a power controller as claimed in claim 15.

19. A receiver for a data communication link, the receiver being configured to process a received signal in substantially real time using repeated implementations of substantially the same first data processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element, the receiver including a control processor coupled to an instruction memory storing processor implementable instructions, the instructions comprising instructions for controlling the receiver to:

repeatedly implement said first data processing element;

adjust the number of repetitions of said implementation; and

jointly control said clock frequency and a power supply voltage to said first data processing element in accordance with said adjustments to control power consumption of said receiver.

20. A receiver as claimed in claim 19, further comprising:

a subsequent data processing element configured to input data from said repeated implementations of said first data processing element; and

an elastic store to store data from said repeated implementations of said first data processing element for asynchronous provision to said subsequent data processing element.

21. A receiver as claimed in claim 19 wherein said receiver is a rake receiver and said first data processing element comprises at least a time multiplexed correlator for said rake receiver, preferably a time multiplexed rake finger for said rake receiver.

22. A data carrier carrying processor implementable instructions for use with a receiver for a data communication link, the receiver being configured to process a received signal in substantially real time using repeated implementations of substantially the same first data processing element, a rate of said repetitions being determined by a clock frequency of said first data processing element, the receiver including a control processor coupled to an instruction memory for storing processor implementable instructions, the processor implementable instructions comprising instructions for controlling the receiver to:

repeatedly implement said first data processing element;

adjust the number of repetitions of said implementation; and

jointly control said clock frequency and a power supply voltage to said first data processing element in accordance with said adjustments to control power consumption of said receiver.